

Data Input/Output Board

KSPT Model IO 21000

The KSPT Model IO 21000 Board is a high performance data interface and processing board supporting data rates up to 1 Gbit/s.

It performs frame level processing of one or two data channels, including frame synchronisation, derandomisation, Reed-Solomon decoding, CRC error detection, time tagging, and data quality annotation.

The KSPT Model IO 21000 is designed for:

- Real-time data ingest and data processing
- Hardware accelerated offline processing
- Data output to external interfaces (test data generator - not supported in current version)

Being fully FPGA based, the IO 21000 is also a very powerful general purpose processing platform for custom defined functions. Its serial and parallel interfaces allow direct board-to-board interconnections, supporting a very modular and powerful system design approach.

Features

- CCSDS AOS compliant
- Supports non-CCSDS data formats
- 64bit / 133MHz PCI-X expansion board
- Selectable input levels on order
- True dual channel operation
- Supports input bit-merging or splitting
- Flexible frame synchronisation
- PN derandomisation
- CRC checking
- Reed-Solomon forward error detection and correction
- Capability for quality and time appending to frames
- Periodic updates of processing status
- All board functions programmable via PCI-X bus
- Accumulated status for data quality statistics
- Internal looping from host / back to host for hardware acceleration
- Direct board-to-board interfaces for system expansion
- In-system upgradability via FPGA image files (software defined)



BOARD AND CONNECTORS

Size

- Full length PCI expansion board

PCI interface

- 64 bits/133 MHz/PCI-X signalling environment
- Intel IOP321 I/O Processor

External interfaces:

Fully supported

- Input data and clock - 2 channels: 8 x SMA
- External clock input: 2 x SMA (MCX)
- Direct board-to-board data transfers: Dedicated header connectors
- Mezzanine board connector for future instalment of other KSPT hardware modules

Full functional support currently not provided

- Output data and clock (for future data output support) - 2 channels: 8 x SMA (MCX)
- IRIG B input: MCX connector
- IRIG B output (daisy chained option): MCX connector
- Ethernet: RJ45

Power

- Below 25 W regardless of input data rate

INPUTS

Input options

- Single input from either channel
- Merging both channels

Data rates

- Single channel in use: Up to 1 Gbit/s
- Both channels in use: Up to 1 Gbit/s total

Input code

- NRZ-L, NRZ-M or NRZ-S

Data polarity

- Normal/Inverted

Note:

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Data alignment

- MSB first in data stream
- Little/big endian conversion option

Input levels

Fixed configuration specified at purchase (Differential ECL default)

- Differential ECL (single-ended possible for low rates)
- LVDS
- RS-422
- Differential TTL (single-ended possible for low rates)

Clock input phase

- 0° or 180°
- Self adjusting clock phase capability

Clock duty cycle

- 50% ± 10%

FRAME SYNCHRONISER

Sync options

- CCSDS AOS/PT, TDM

Sync pattern

- Programmable up to 64 bits

Bit error tolerance

- Allowing up to 31 bit errors

Frame length

- Programmable up to 64 kbytes

Sync strategy

- Search-Check-Lock - up to 15 frames
- Lock-Flywheel-Search - up to 15 frames

Bit slip tolerance

- Up to ± 4-bits

Operational modes

- Fixed frame length
- Variable frame length
- Adaptive (fixed but unknown) frame length
- Asynchronous blocking of data (no synchronisation)

PN DERANDOMISER AND CRC CHECKER

PRN derandomiser

- Fully programmable derandomiser

CRC error checker

- CCSDS recommended polynomial: $g(x) = x^{16} + x^{12} + x^5 + 1$
- Fully programmable offsets

FORWARD ERROR DETECTION AND CORRECTION

R-S decoding

- CCSDS-recommended Reed-Solomon codes: R-S (255, 223); R-S (255, 239); R-S (10, 6)
- Codewords length from 33 to 255 bytes
- Automatic de-interleaving from 1 to 16 codewords
- Filtering of uncorrectable frames

QUALITY AND TIME APPENDING

Frame sync status

- Up to 8 bytes appended to the frames

R-S status

- Up to 32 bytes including frame counter, error status, and user defined fields appended to the frames

Time-stamping - 6 bytes time field:

- Day of year; millisec of day; microsec. of millisec

PERIODIC

PROCESSING STATUS

- Periodic dump of accumulated processing status from frame synchronisation and forward error detection and correction

OUTPUTS

Full data output function will be supported in future versions of the board – currently only the physical level is available!

Output levels

Fixed configuration specified at purchase (Differential ECL default)

- Differential ECL
- LVDS
- RS-422

FUTURE FEATURES – depending on demand:

- Automatic data detection and input selection
- Automatic data ambiguity resolving
- Viterbi decoding
- Time values: IRIG B input and output
- Serial data output
- Direct board-to-board data transfers
- 10 Mbps / 100 Mbps / 1 Gbps Ethernet interface

More functionality may be made

